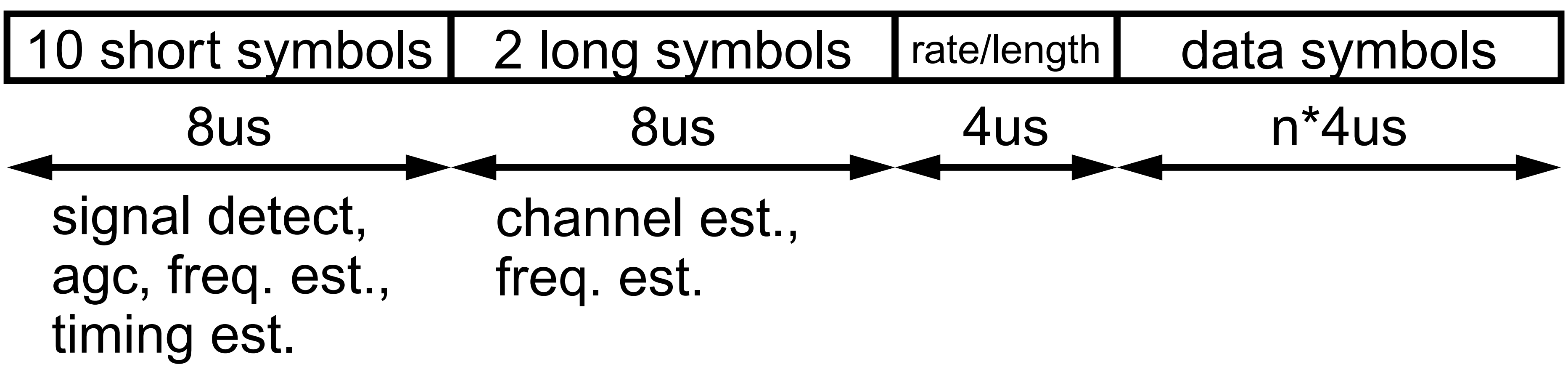
Outline

- 802.11a Overview
- Medium Access Control Design
- Baseband Transmitter Design
- Baseband Receiver Design
- Chip Details

What is 802.11a?

- IEEE standard approved in September, 1999
- 12 20MHz channels at 5.15 - 5.35 GHz and 5.725 - 5.825 GHz
- Coded OFDM with 48 data and 4 pilot subcarriers. Coding rate = {1/2, 2/3, 3/4}. Modulation = {bpsk, qpsk, 16qam, 64qam}
- Data rate: 6Mb/s - 54Mb/s per channel
- Symbol Format:

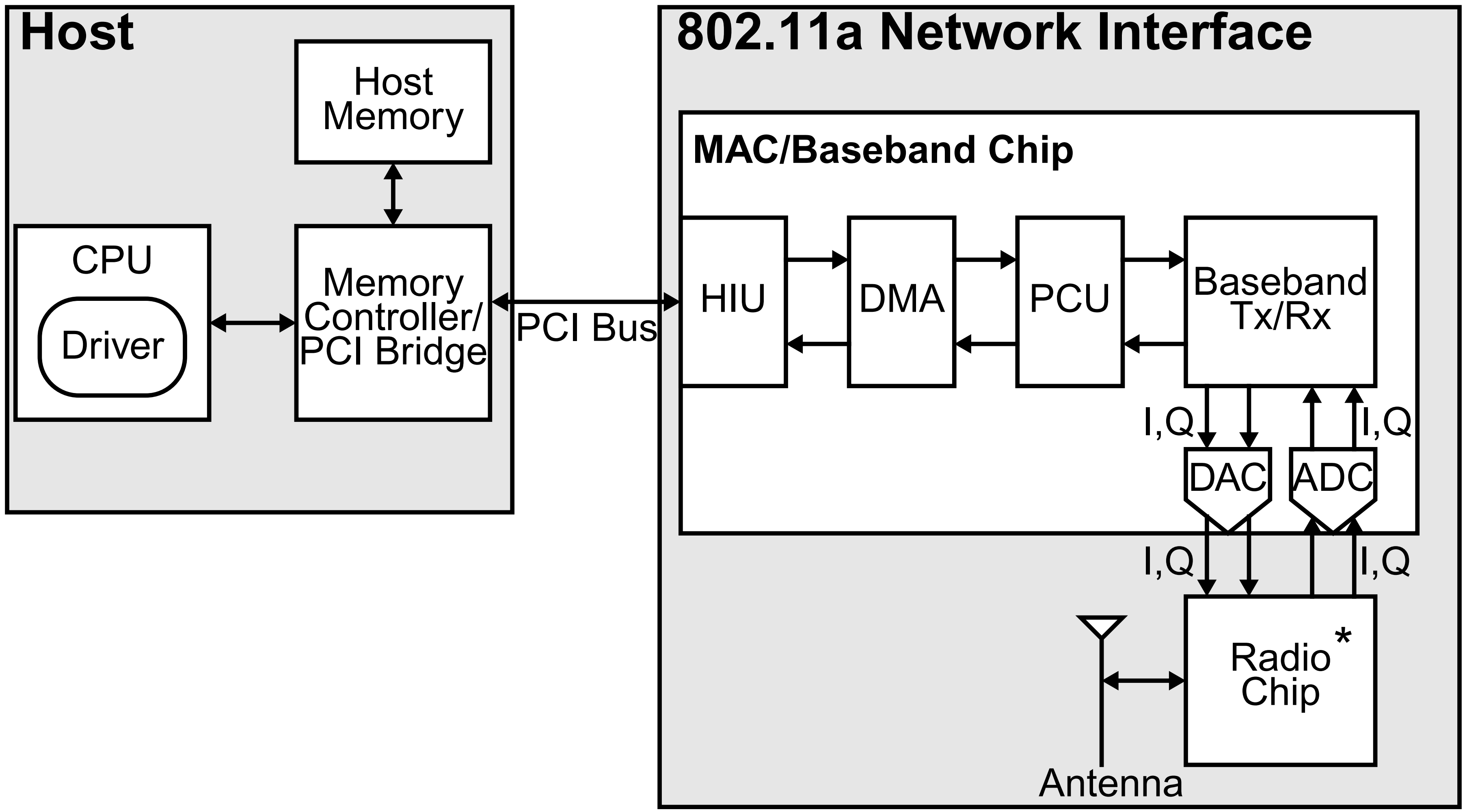


Why 802.11a?

Compared to 802.11b:

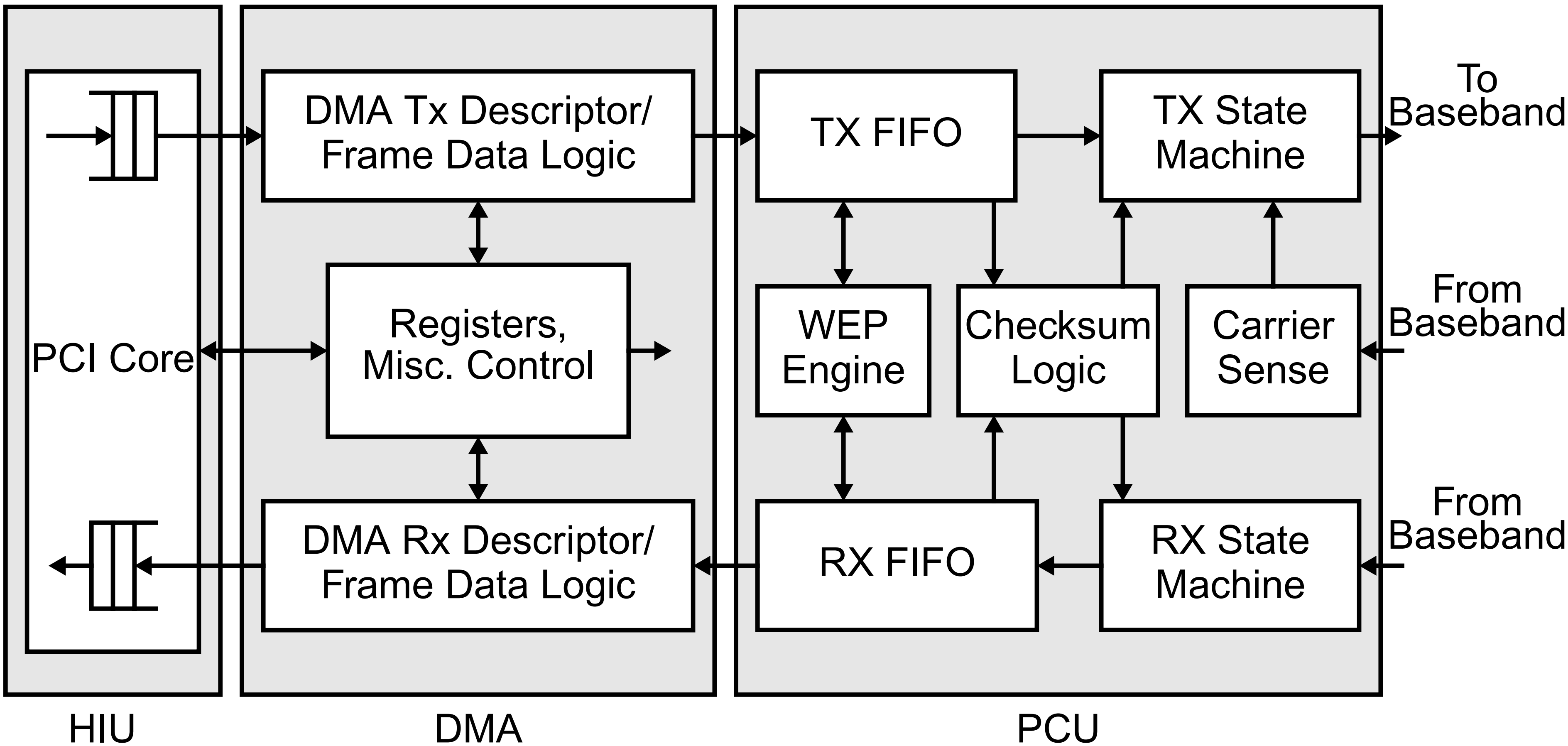
- higher data rate per channel (peak of 54Mb/s vs. 11Mb/s)
- measured throughput is 2 to 5 times higher in a typical office environment
- more non-overlapping channels (12 vs. 3) implies less co-channel interference
- the result is ~10x higher system capacity, accommodating more users or enabling lower deployment costs
- 5GHz bands have less interference (2.4GHz has 802.11b, HomeRF, Bluetooth, cordless phones, microwave ovens ...)
- less energy per bit transferred

System Overview



* D. Su, et al., ISSCC 2002, Paper 5.4

MAC Architecture



MAC Partitioning

Partitioning is based on required timing.

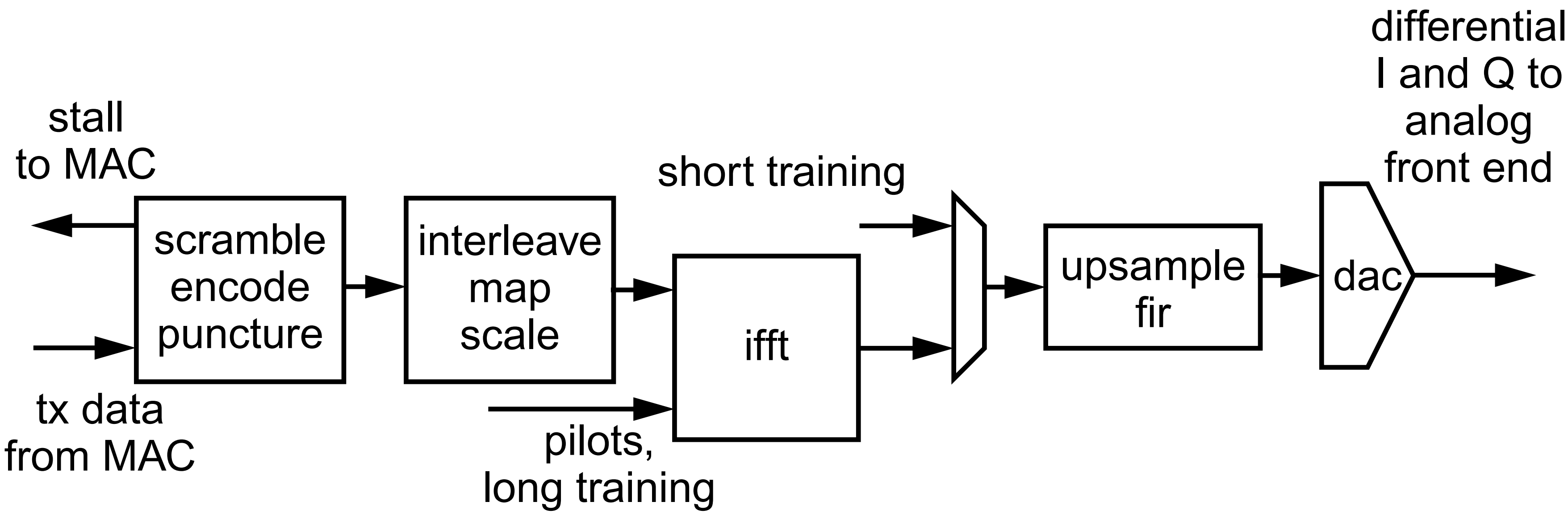
Timing-critical functions:

- demand fast response or precise timing. Managed by the PCU.
- include CRC generation and checking, hardware-level frame retry, channel access, timer updates, and generation of special frames such as beacons, ACK, CTS

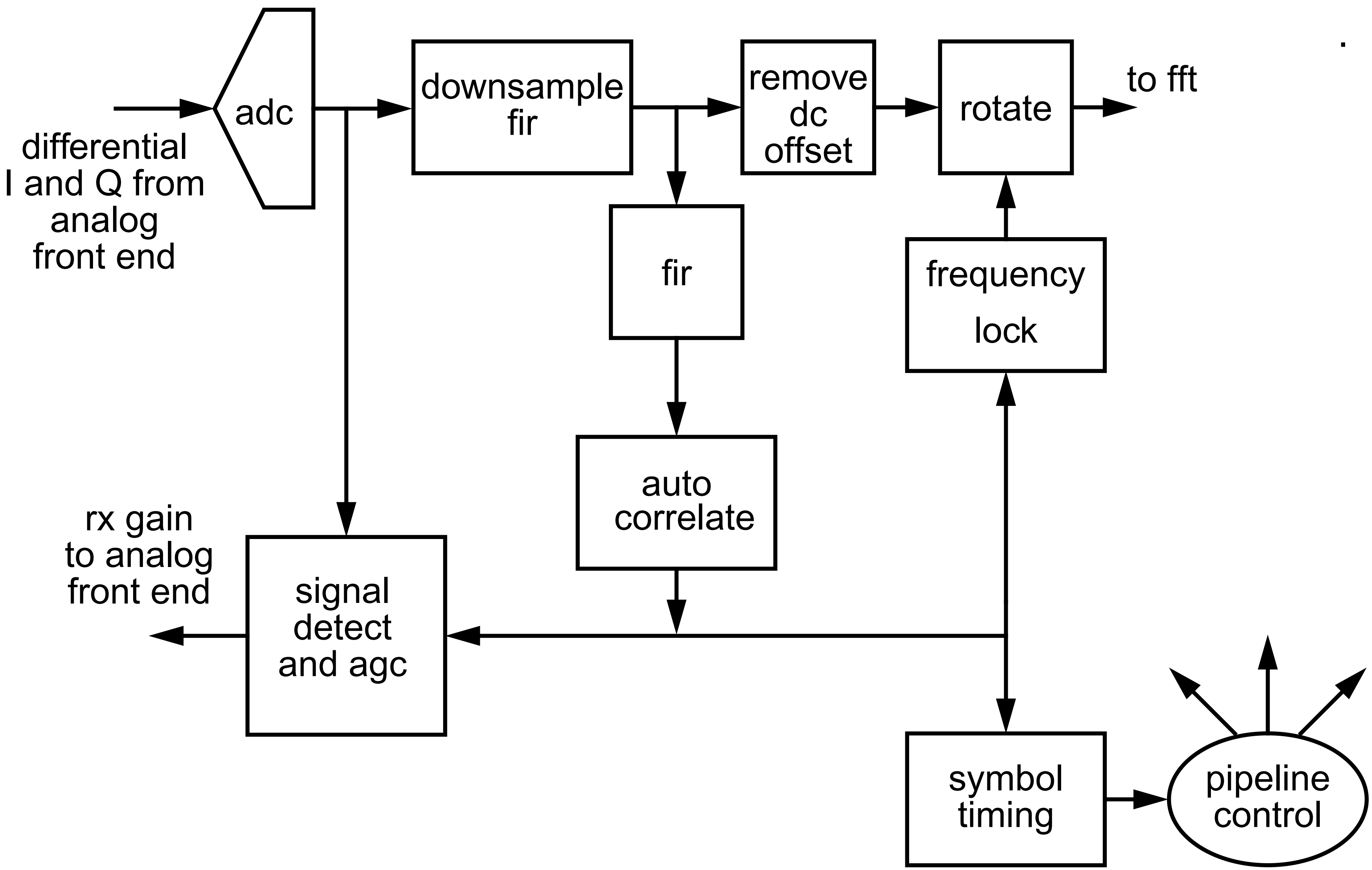
Non-timing-critical functions:

- performed in the driver software executing on the host
- include complex frame exchanges (e.g.: authentication and association), fragmentation, frame buffering and bridging, and other network management functions

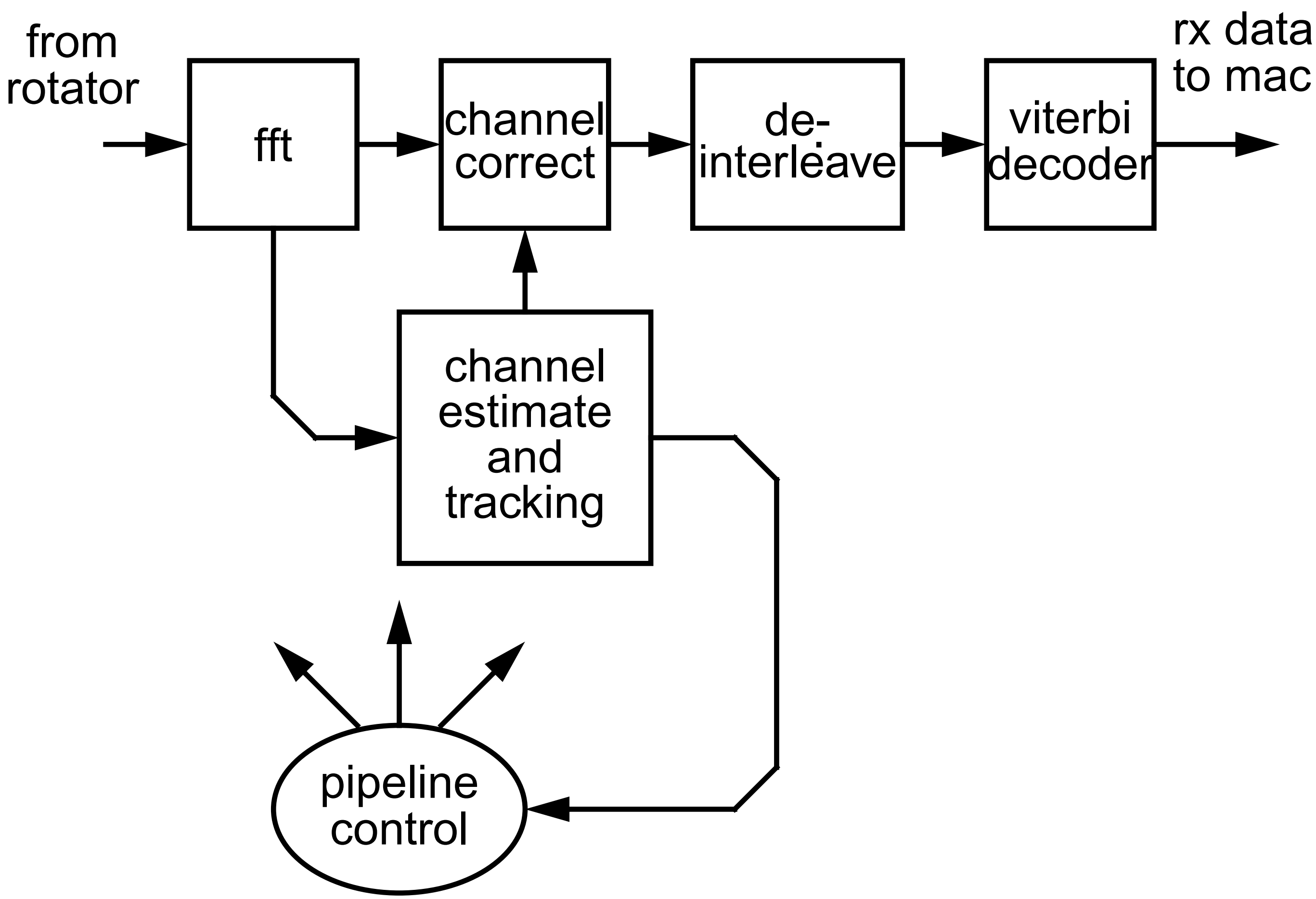
Baseband Transmitter



Baseband Receiver



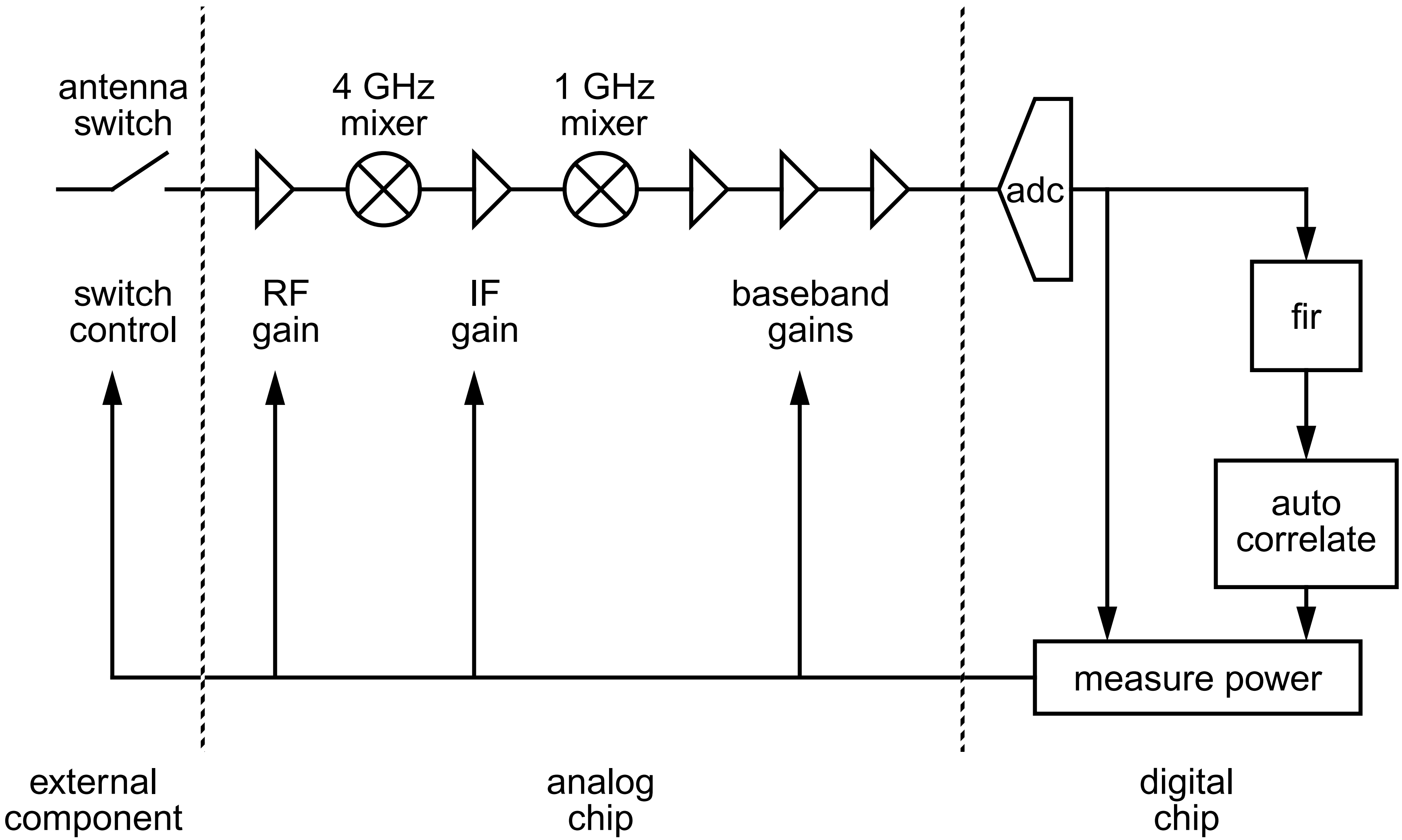
Baseband Receiver (cont)



Signal Detection and Automatic Gain Control

- need to detect ~60dB range of received signal strength
- may require multiple power measurements and gain changes within ~4us
- for weak signal detection, auto-correlated power is measured with a period of 0.8us (short symbol duration)
- for strong signal detection, raw power is measured, especially saturation at the ADC
- the goal is to maximize signal size at the ADC while providing headroom for adjacent channel interference and the peak-to-average-ratio of OFDM symbols

AGC Loop


antenna switch
4 GHz mixer
1 GHz mixer
adc
switch control
RF gain
IF gain
baseband gains
fir
auto correlate
measure power
external component
analog chip
digital chip

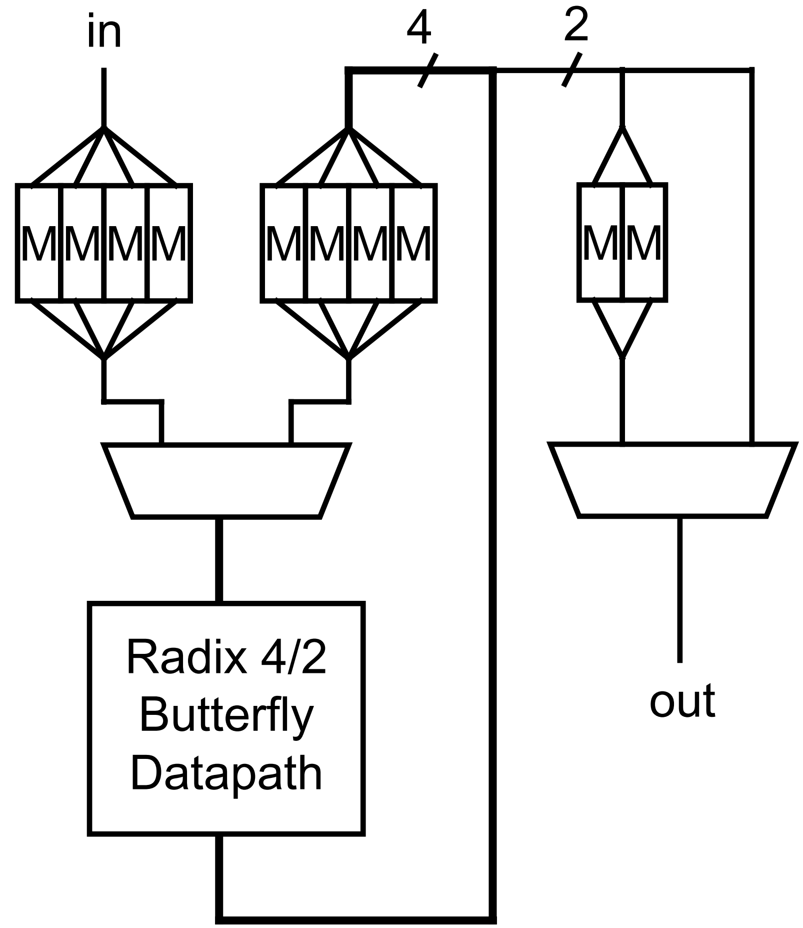
Fast Fourier Transform

128-pt FFT reduces adjacent channel filtering requirements and preserves the guard interval

time-multiplexed radix 4/2 butterfly datapath

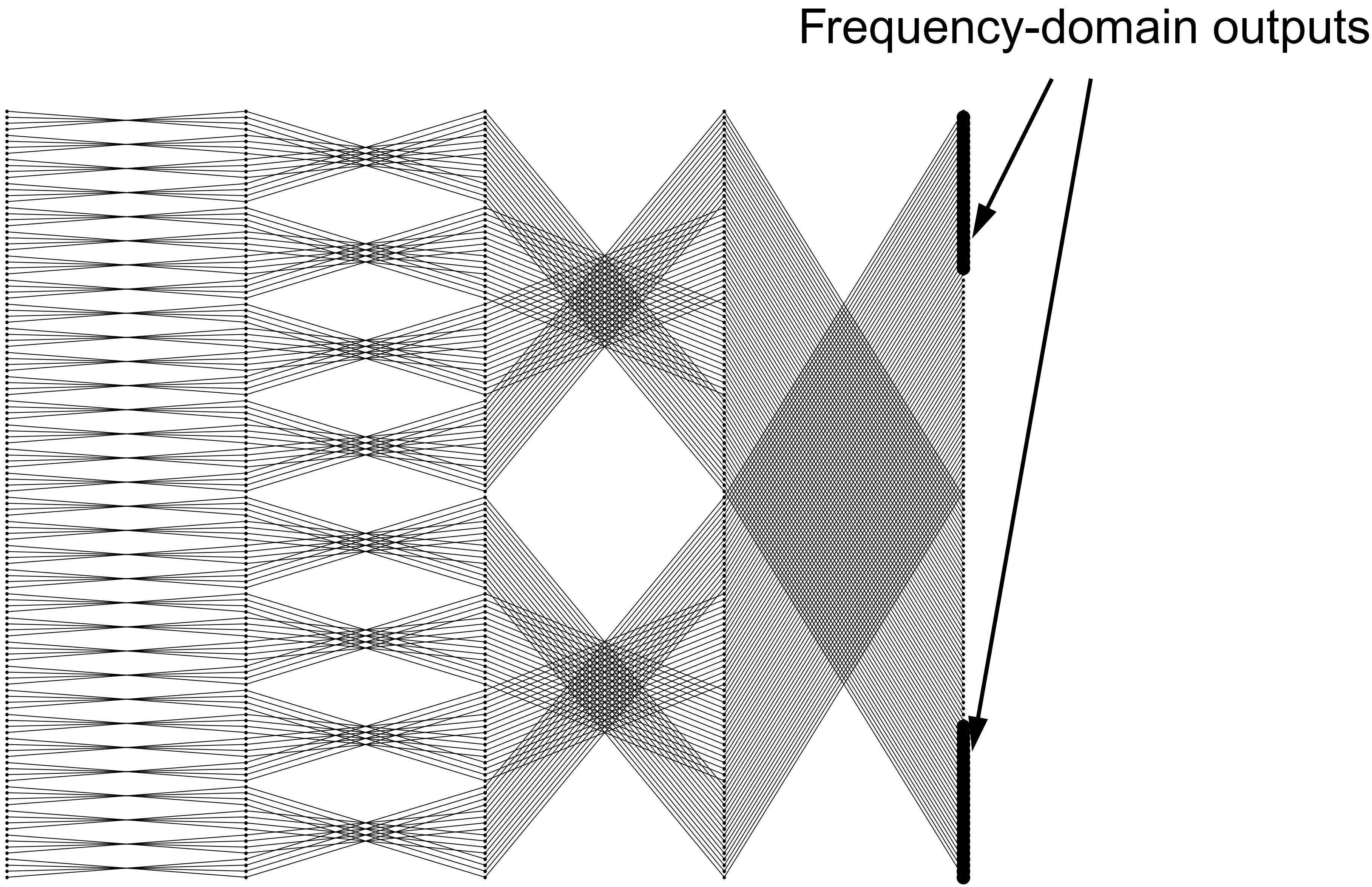
contains memory for input, temporary storage and output

shares hardware with the IFFT

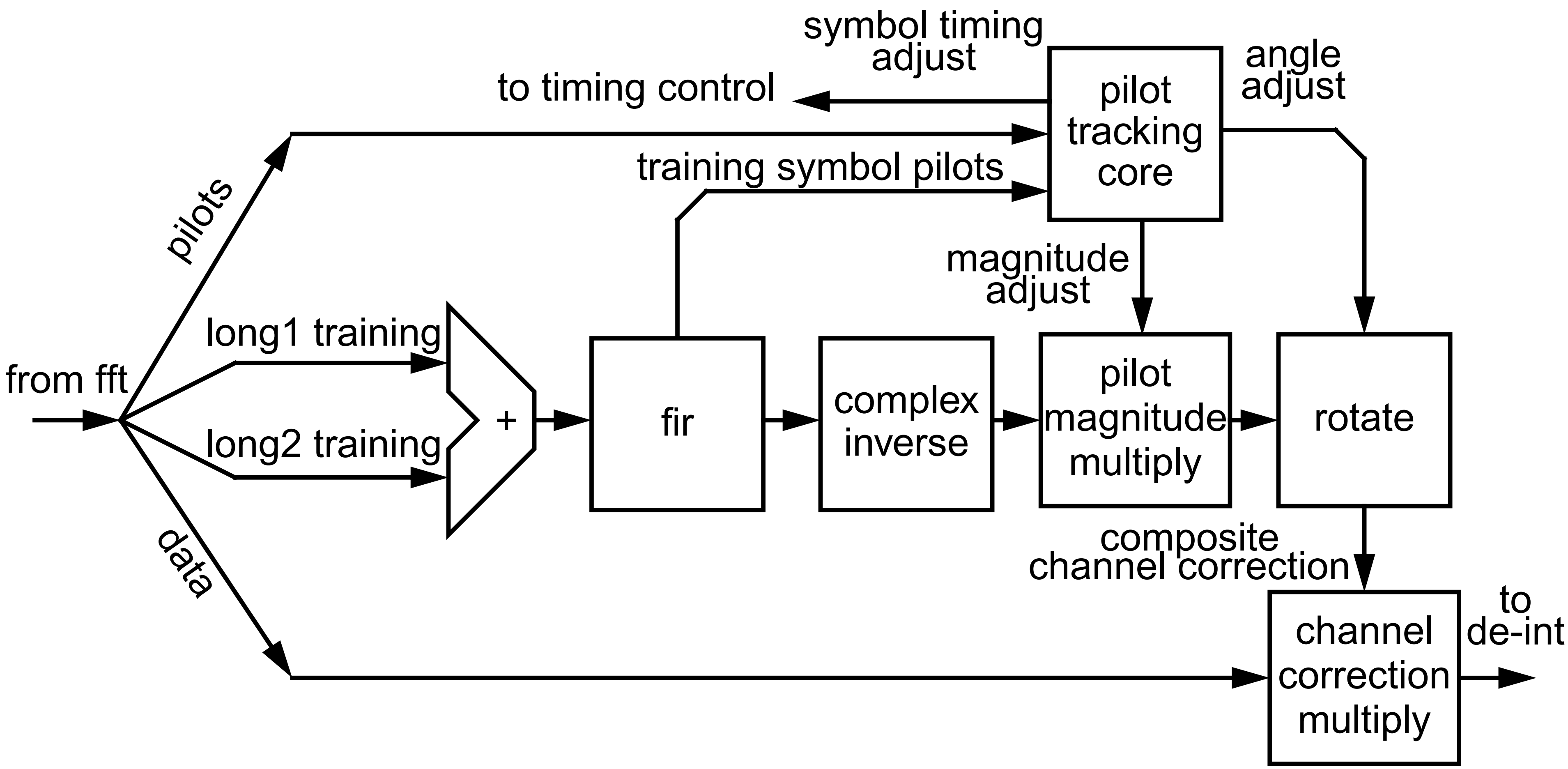


M = single-ported memory

FFT RX Butterfly Diagram

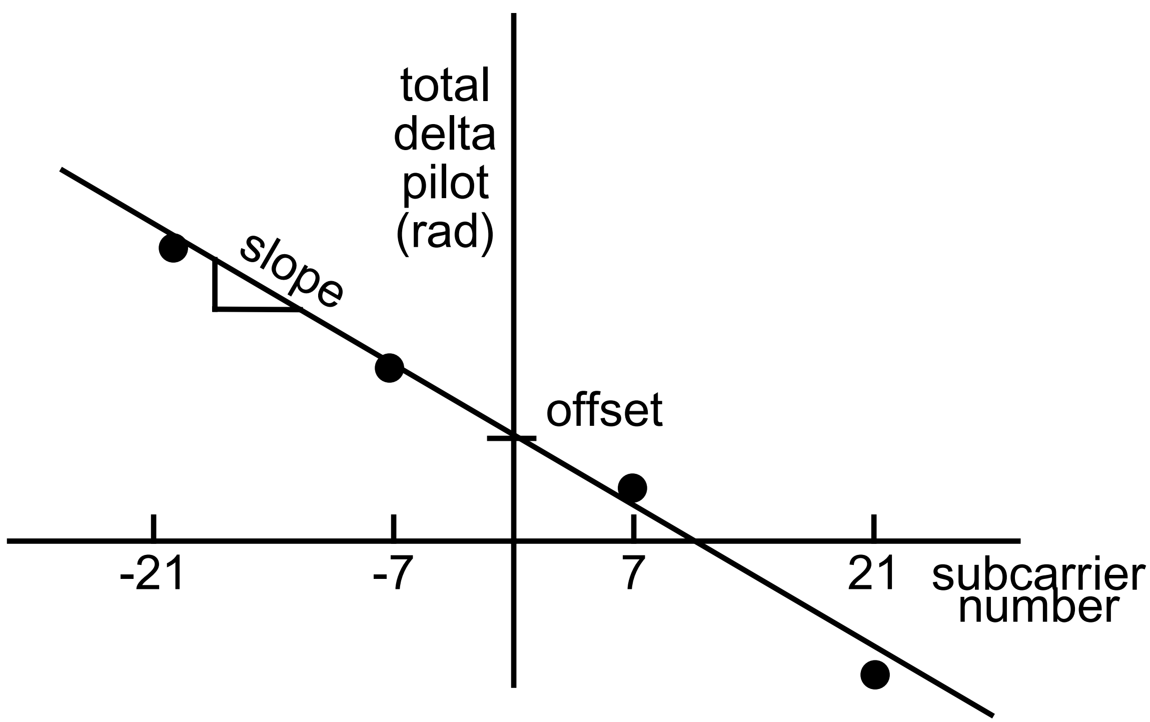


Pilot Tracking and Channel Correction



Pilot Phase Tracking

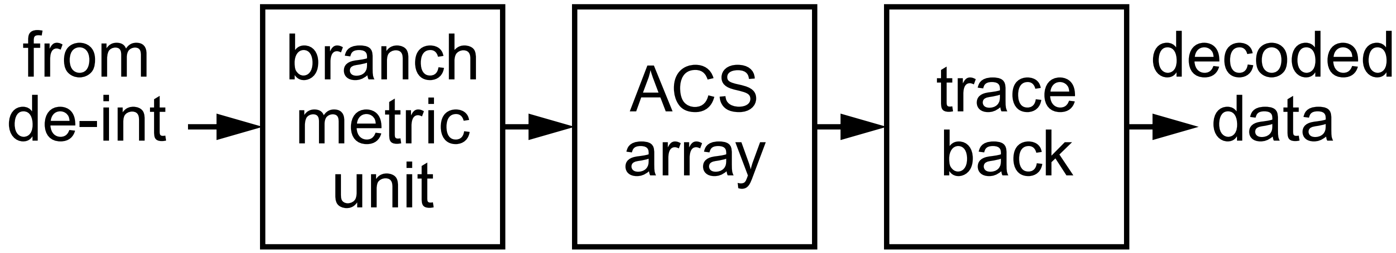
- for each data symbol, for each of the 4 pilots, track total change in phase compared to the training symbols
- perform a least squares fit to determine phase correction for each data subcarrier



Pilot Tracking (cont)

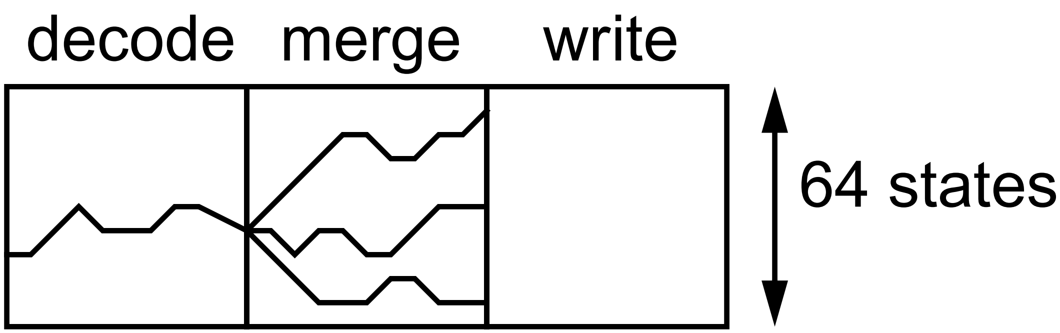
- adjust channel estimates to account for frequency estimation error, phase noise and symbol timing drift
- drift in offset indicates frequency estimation error. Apply to rotator before FFT to reduce inter-carrier interference
- drift in slope indicates a shift in symbol timing. As slope becomes steeper, adjust symbol timing later. As slope becomes flatter, adjust symbol timing earlier
- pilot magnitude tracking monitors amplitude variations by comparing pilot power in the training symbols to pilot power in the data symbols

Viterbi Decoder



- branch metric unit computes soft trellis weights from the decoded constellations
- add-compare-select (ACS) array is radix-4, fully parallel

traceback memory partitioned into three rotating buffers



Power Management

Sleep:

- the chip can be programmed to sleep automatically and awake just before the next beacon
- the PCU parses the beacon to determine whether to remain awake for additional frames or re-enter sleep. Host interaction is required only if additional frames are to be processed.

Design Optimization:

- streamlined design, especially for datapaths
- MAC implemented with dedicated logic (yet still highly flexible), requiring no off-chip RAM or program storage
- aggressive clock gating

Chip Details

Technology	Standard 0.25u CMOS, 5 layer metal, 2.5V core, 3.3V I/O
Transistor Count	4.0M
Die Size	6.8 mm x 6.8 mm
Package	196-pin BGA
Power at 54Mb/s (Tx/Rx)	
Core	219 / 203 mW
DACs + supporting circuitry	68 / 0 mW
ADCs + supporting circuitry	0 / 211mW
I/O	25 / 24 mW
PLL	14 / 14 mW
Total	326 / 452 mW

Die Photograph