ADVANCE PROGRAM

HOT CHIPS 20

A Symposium on High-Performance Chips
August 24-26, 2008, Memorial Auditorium,
Stanford University, Palo Alto, California

HOT CHIPS brings together designers and architects of high-performance chips, software, and systems. Presentations focus on up-to-the-minute real developments. This symposium is the primary forum for engineers and researchers to highlight their leading-edge designs. Three full days of tutorials and technical sessions will keep you on top of the industry.

Sunday August 24

Morning Tutorial ***High Bandwidth Memory Technology & Systems Implications***
Chuck Moore **AMD** (others TBA)
Craig Hampel **Rambus**

Afternoon Tutorial ***Scalable Parallel Programming with CUDA***
Ian Buck, Michael Garland, Patrick Legresley, Massimiliano Fatica **NVIDIA**
Wen-mei Hwu **Univ. of Illinois**

Monday August 25

Multi-Core Technologies
- MicroNetwork-Based Coherency: Extending Coherency over Standard Networks **3Leaf Sys.**
- The Roofline Model: A tool for Auto-tuning Kernels on Multicore Architectures **UC Berkeley**
- Power-Performance Comparison of POWER5 &POWER6 Microprocessors **IBM**

Keynote 1 **Sebastian Thrun**
- ***Cars that drive themselves*** **Stanford**

Video & Media
- SpursEngine - Cell Derivative High-Perf Stream Proc. for Media Acceleration **Toshiba**
- A 167-processor Array for Efficient DSP & Embedded Apps Processing **UC Davis**
- PNX5100 System Arch & Apps: A High-Perf. Full HD 120Hz Engine **NXP Semi.**
- AMD mediaDSP: A Programmable Multicore Video Processor Platform **AMD**

Mobile Media Processing
- A 300-mW Single-Chip NTSC/PAL Television for Mobile Applications **Telegent**
- Voice Processor Based on Human Hearing System **Audience**
- NVIDIA APX2500: Enabling Stunning Handheld Graphics & HD Video **NVIDIA**

Supercomputing
- PowerXCell 8i: A Cell Broadband Engine Architecture for Supercomputing **IBM**
- A Specialized ASIC for Molecular Dynamics **D.E. Shaw**

Panel **Ready, Fire, Aim - 20 years of hits & misses at Hot Chips** **Nick Tredennick**
Nathan Brookwood John R. Mashey David Patterson
Dave Ditzel Howard Sachs Michael Slater

Tuesday August 26

FPGAs
- Virtex-5 FXT, a New Field-Programmable Gate Array Platform **Xilinx**
- MAXware: acceleration in HPC **Maxeler**
- New 40nm High Performance FPGA and ASIC Common Platform **Altera**

PC Chips
- AMD 780G, an x86 Chipset with Advanced Integrated GPU **AMD**
- Micro-architecture of Godson-3 Multi-Core Processor **Chinese Academy of Sciences**
- Inside Intel's Next Generation Nehalem Microarchitecture **Intel**

Keynote2 **Richard Swanson**
- ***SunPower's History and Technology*** **SunPower**

Networking
- Low Cost 200Mbps Broadband Powerline Communications ChipSet **DS2**
- The QFP Packet Processing Chip Set **Cisco**

Visual Computing
- NVIDIA G100: TeraFLOPS Visual Computing **NVIDIA**
- Larrabee: A Many-Core x86 Architecture for Visual Computing **Intel**

Server Chips
- Tukwila: A Quad-Core Intel(R) Itanium(R) Processor **Intel**
- SPARC64VII: Fujitsu's Next Generation Quad-Core Processor **Fujitsu**
- Rock: A 3rd Gen 65nm, 16-Core, 32+32 Scout Threads CMT SPARC Proc. **Sun**

Please visit us on the web: **http://www.hotchips.org**
or drop us a line via Email: **info2008@hotchips.org**

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IEEE computer society

This is a preliminary program; changes may occur. For the most up-to-the-minute details on presentations and schedules, and for registration information, please visit our web site where you can also check out HOT Interconnects (another HOT Symposium being held following HOT CHIPS):

SSCS IEEE

A Symposium of the Technical Committee on Microprocessors and Microcomputers of the IEEE Computer Society and the Solid State Circuits Society