Massively Parallel Processor Array for Mid-/Back-end Ultrasound Signal Processing

Energy Efficient Parallelism

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Many-core chips can take to DSP in radar, sonar, etc.
Thousands of cores in future 65 nm 167-core Piezoelectric ceramic

Basic Ultrasound System

Many-core DSP Architecture

Piezoelectric ceramic

Motion

16 KB Shared Memories

Task Parallelization Example

Algorithm 1: CORDIC Arctangent

Requirements:
1. Initial values of \( I \) and \( Q \) processing

for \( n = 0 \) to \( N - 1 \) do

\[ I_{out} = I + n \]

\[ Q_{out} = Q - n \]

if \( Q > 0 \) then

\[ I_{out} = I - n \]

\[ Q_{out} = Q + n \]

else

\[ I_{out} = I + n \]

\[ Q_{out} = Q - n \]

end if

\[ I = I_{out} \]

\[ Q = Q_{out} \]

\[ \theta = \tan^{-1}(I/Q) \]

end for

\( \theta \) is the angle of the vector between the \( I \) and \( Q \) components

Many-core Energy Efficiency

• Recent interest in portable ultrasound machines
  • Extended battery life desired
  • Performance compromise must be minimal
  • Energy efficiency through parallelism
  • Ultrasound processing similar to DSP in radar, sonar, etc.
  • DSP applications tend to exhibit task-level parallelism
  • Many-core chips can take advantage of parallelism
  • Thousands of cores in future nanometer CMOS technologies

Conclusions

• Mid-/Back-end processing can be done efficiently with a many-core array of simple DSP processors
  • Task level parallelism is ubiquitous in ultrasound signal processing
  • Massive fine-grained parallelism is used to increase energy efficiency by lowering required operating frequencies to maintain throughput
  • Power density is also reduced by loading multiple cores with larger workloads
  • DVFS capability and dithering approach to reach the optimal operating point of each processor as determined by the \( CPF \) and \( CPF2 \): 150.23 mW total average power
  • Average power per frame for B-Mode at 37.6 fps and color flow at 12.5 fps is 1.33 mW/frame and 2.66 mW/frame respectively
  • Compare this to a static two voltage operation with \( VddHigh = 0.8 \) V and \( VddLow = 0.67 \) V, which results in a total average power of 160.37 mW (6.5% increase)

Results

• Assume: 10 MHz carrier frequency, decimation factor of 4, and 80 Msamples/sec ADC, with pulse repetition frequency of 19.25 KHz

512 B-mode beam lines, 192 color flow beam lines, manageable size of 8 ~ 1024 samples per beam line

• Requires: 77 DSPs, 6 shared memories, and one FFT processor

• Cycles per FIFO read (CPF) and cycles per FIFO write (CPF2) used to determine the required operating frequencies for each processor

• Optimal Vdd & frequency average power results approximates the performance of voltage dithering

Many-core DSP Architecture

• 164 Simple DSP processors
  • 3 Dedicated-purpose DSP processors
  • 3 Shared memories
  • Long-distance circuit-switched communication network
  • Dynamic power and frequency scaling (DVFS)
  • Per-core digitally programmable ring oscillator
  • Two power states
  • VddHigh and VddLow

Each core only contains a 128-bit DMem and a 128-bit 16-bit IMem.

FIFOs used for interprocessor communication

Voltage Dithering (cont.)

• Workload ~ frequency, \( f_0 = \) desired workload
  • At VddHigh, maximum frequency = \( f_0 \)
  • At VddLow, maximum frequency = \( f_0 \)
  • Duty Cycle: \( P_{d} = (f_0 - f_0)/f_0 \)
  • \( P_{d} = 1 - P \)

VddHigh = 1.3 V, \( f_0 = 1.2 \) GHz
VddLow = 0.9 V, \( f_0 = 0.8 \) GHz

Ideal case: \( P_{d} = 72.22 \% \), \( P_{d} = 27.78 \% \)

Measured: \( P_{d} = 74.4 \% \), \( P_{d} = 25.6 \% \)

Energy Efficient Parallelism

• Many-core processors can take advantage of parallelism

128 core array of simple DSPs

128-word DMem and a 128-bit 16-bit IMem

Mid-/Back-end Implementation

Task Parallelization Example

Many-core Energy Efficiency

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• DVFS capability and dithering approach to reach the optimal operating point of each processor as determined by the \( CPF \) and \( CPF2 \):

\( \text{Average Power} = \frac{1}{1024} \cdot \sum_{i=1}^{1024} \frac{P_{d}}{P_{d}} \)