A Band-Gap Reference with Internal Digital Signal Processing

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***Abstract*—The objective of this project is to design a low-power band-gap voltage reference that uses internal digital processing to compute its analog output. A conventional band-gap reference creates an output voltage by summing a with a constant times in the analog domain. The idea of this project is that digitizing the and voltages allows the arithmetic to be done in the digital domain, which may be less expensive in die area and power dissipation than using standard analog techniques in modern CMOS processes.**

I. Introduction

The overall system is composed of two generators, an analog to digital converter (ADC), a FIR filter, a digital to analog converter (DAC) and some arithmetic logic units (ALUs). In Figure 1, two V_{BE} voltages are created by pushing currents $I_{C1}$and I_{C2} into bipolar junction transistors (BJTs). A random signal (dither) is added on top of each V_{BE} with a value $\geq 1LSB$.

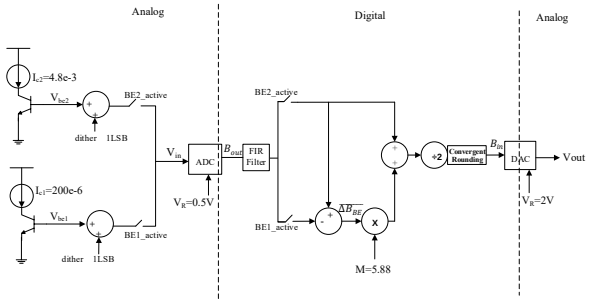

Fig. 1. Top level system diagram of band-gap referenced ADC and DAC

Because one ADC makes both measurements, $V_{BE1} + dither$ and $V_{BE2} + dither$ alternate as the ADC input, V_{in}.

II. ADC Design

Since the goal is to create a band-gap reference with low temperature coefficient, speed is not of great concern. A good candidate for the ADC design is a dual-slope A/D converter as shown in Figure 2. Although these converters are slow, they can have high accuracy, which is desired in the system under investigation. The high accuracy comes from the fact that the dual slope ADC is doing indirect analog to digital conversion. The input voltage is converted to another analog voltage (the integrator output) and then converted to a digital output, ideally providing no dependence on component matching. A switched capacitor implementation is chosen for the integrator rather than a RC topology because capacitors are the best passive components in most CMOS processes.

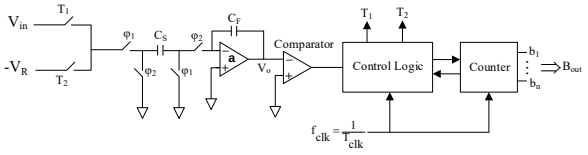

Fig. 2. Dual-Slope ADC model

In Figure 2, V_{in} is integrated for a fixed time $T_1 = 2^N T_{clk}$, creating a negative integrated output for $V_{in} > 0$. During T_2, $-V_R$ is integrated, causing the integrated output to increase back toward zero with a fixed slope. A counter runs until the integrator voltage crosses 0, at which point the final value of the counter is B_{out}; correspondingly $T_2 = 2^N B_{out} T_{clk}$. Since two integrations are done using the same components, $B_{out} = \frac{V_{in}}{V_R}$with no dependence on components as long as the component values are constant and the op amp gain is infinite during T_1 and T_2.

The ADC is run repeatedly, and its outputs are averaged using a FIR filter. This is done for both V_{BE1} and V_{BE2}. In the digital domain, $\overline{\Delta B_{BE}}$(digitized $\overline{\Delta V_{BE}} = \frac{\overline{V_{BE2}} - \overline{V_{BE1}}}{V_R}$) is created by subtracting $\overline{B_{BE2}}$(digitized $\overline{V_{BE2}} = \frac{\overline{V_{BE2}}}{V_R}$) from $\overline{B_{BE1}}$(digitized $\overline{V_{BE1}} = \frac{\overline{V_{BE1}}}{V_R}$). Next $\overline{\Delta B_{BE}}$ times a scaling factor M is added back to $\overline{B_{BE2}}$ to create a digital version of the band-gap voltage reference. The digital reference has one bit more resolution than each of the ADC outputs since it is the summation of $\overline{\Delta B_{BE}} * M$ and $\overline{B_{BE2}}$, where M is a scaling factor (see appendix for more information on M). This value is divided by 2 to reduce the resolution requirement on the DAC thereby matching the ADC resolution. Convergent rounding is done after the division to avoid biasing the divided value. B_{in} is the output of the rounding operation that gets sent to the DAC.

III. DAC Design

Figure 3 shows the proposed dual-slope DAC. During T_1 the DAC calibrates a digitally controlled analog integrator by running a counter for 2^N clock cycles while integrating V_R. At the end of T_1, V_{out} is compared to V_R. Ideally the input and target output should be identical during calibration. If $V_{out} > V_R$, the gain of the integrator is reduced by 1 LSB. Similarly, if $V_{out} < V_R$, the gain of the integrator is increased by 1 LSB. Then T_1 is repeated a number of times until the gain is adjusted such that $V_{out} \cong V_R$ after which the DAC stops adjusting the gain. On T_2, integration is performed on V_R for $2^N B_{in}$clock cycles to create the desired band-gap voltage reference V_{out}. The DAC implementation avoids using a sample and hold because the integrator is setup to hold V_{out}at the end of T_2. A "Freeze" signal from the control logic stops the integration by disconnecting and setting the integrator input to ground.

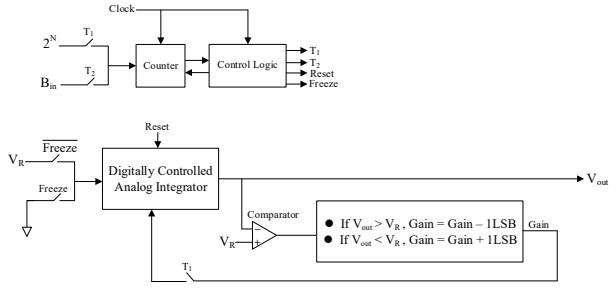

Fig. 3. Dual-Slope DAC model

The most common topology for this integrator is a switched capacitor based topology. The downside to using this topology without modifications are that when the integrator samples ground and transfers the resulting change, the op-amp offset will continue to be integrated causing another error.

IV. Non-idealities

A. ADC

Some issues of interest in the ADC design are comparator and op-amp non-idealities. One of the advantages of using a dual-slope ADC is that it is highly tolerant to comparator offset. When the integrator integrates $-V_R$, its output moves back toward zero. When the integrator output crosses the comparator threshold, including offset, the integrator stops integrating. As a result, the integrator output starts and stops from the comparator offset in subsequent cycles, and comparator offset does not affect the ADC output if the integrator is ideal.

In the case of the op-amp, there are two main non-idealities to consider: op-amp offset and finite gain error. Op-amp offset causes ADC offset and ADC gain error. These errors occur because the integrator input is connected to either the input voltage or the reference voltage on each of the phases. When the op-amp is connected to the input voltage, the op-amp offset causes the integration to depend on both the input and the offset. This is a constant error, which leads to an ADC offset error. During the second phase, the op-amp offset causes the slope of the integration to depend both on the reference voltage as well as the offset. This error changes the full scale voltage, which creates an ADC gain error.

Finite gain error of the op-amp causes ADC non-linearity. With finite op-amp gain, the voltage at the op-amp negative input terminal is driven by negative feedback to $-\frac{V_o}{a}$. This nonzero value causes some charge to remain on C_S instead of being transferred to C_F. As a result, the integrator step size is dependent on the integrator output, causing the ADC to be nonlinear. For 12-bit resolution, the op-amp gain must be at least 200,000 to make this error insignificant.

B. DAC

The biggest non-ideality in the DAC comes from the integrator "freezing" V_{out}. The output voltage may not necessarily stay at the desired value because of integrator leakage. The rate at which the DAC produces a new output will affect the amount of leakage. Also, repeated integration of the op-amp offset will change the band-gap voltage, so an integrator with very low op-amp offset is desired. Input or output offset cancellation techniques may need to be applied to reduce this error.

V. Optimizations and Figure of Merit (FOM)

The initial simulations show that a high resolution (15-16 bits) is needed in generating the band-gap reference. One way this resolution requirement is reduced is by division and convergent rounding. The digitized band-gap voltage corresponds to summing a scaled $\overline{\Delta B_{BE}}$ to $\overline{B_{BE2}}$, which produces a reference has one bit more resolution than each of the ADC outputs. If there is no optimization, the DAC would require one bit higher resolution than the ADC. This resolution requirement on the DAC may be reduced by 1 bit dividing the output codes from the ADC by 2 and then rounding to the nearest even integer (convergent rounding). Another optimization implemented is adjustment of the ADC V_R level to match the range needed by the input. For the temperature range being considered (-55^oC to 125^oC), the generated V_{in} is between 0.5 V-1 V, which is less than half of a full scale voltage for $V_R = 1$ V. For a good accuracy ($TC < 20\frac{ppm}{^oC}$ where TC is defined later) , a high resolution (> 12 bits) is needed to convert this small range of inputs. This requirement may be reduced by lowering the full scale voltage to match the input range (i.e. $V_R = 0.5$ V). In this project, by reducing the full scale range by a half, the resolution requirement is lowered by 1bit since only half of the original range is required for conversion.

Dithering is implemented as a way of further reducing the resolution requirement. A random input signal is added on top of each of the V_{BE}s. The corresponding digital outputs are passed through a FIR filter at the ADC output. The FIR filter averages samples from the outputs of the ADC. To show dithering and averaging reduces the resolution requirement

consider the following: for simplicity, assume that the quantization error of the ADC is between 0 and 1 LSB. Then an additive random dither signal at the ADC input between 0 and 1 LSB causes the ADC output to sometimes increase by one code, and the probability that this increase occurs is proportional to the quantization error. As a result, averages after quantization with additive dither can allow the ADC to resolve signals smaller than 1 LSB, reducing the resolution required in the system.

In order to quantify the performance of the system, a figure of merit (FOM) is defined as:

$$TC = \frac{1}{V_{out}} * \frac{V_{outmax} - V_{outmin}}{T_{max} - T_{min}}$$

Where $V_{out} = 1.25$ V is the band-gap voltage. For the military range, $T_{max} = 125^oC$ $T_{min} = -55^oC$. For commercial applications, $T_{max} = 70^oC$ $T_{min} = 0^oC$. V_{outmax} and V_{outmin} are the maximum and minimum band-gap outputs for any temperature between T_{max} and T_{min}, respectively. The FOM for an all-analog implementation is $TC_{military} = 13.37\frac{ppm}{^oC}$ for the military range and $TC_{commercial} = 8.58\frac{ppm}{^oC}$ for the commercial range.

VI. Simulation Results

Figure 4 is generated given the following parameters: dither = 1 LSB, FIR filter length = 5 samples, and infinite gain on the op-amps. The top three graphs show V_{out} versus temperature of the DAC for 11-13 bit resolutions. The red lines correspond to the voltage reference of an all analog implementation. The FOM versus resolution is plotted on the fourth graph. The general trend is that the FOM approaches the analog implementation with increasing resolution.

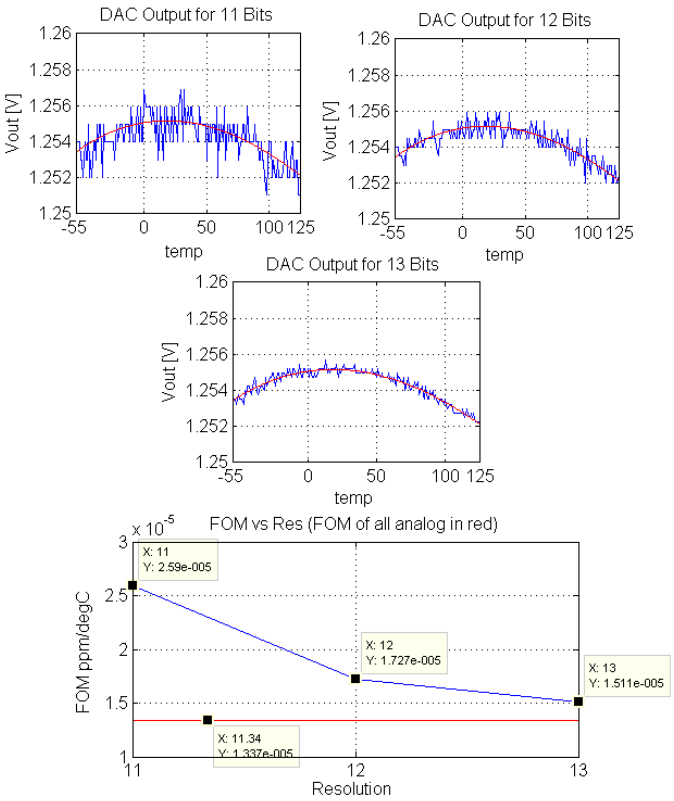

Fig. 4. Output simulation results for dither = 1 LSB and FIR=5 sample averaging

Table I shows the relationship between the length of the FIR filter and resolution change. For a given resolution, its FOM approaches an analog FOM with increasing FIR length. Figure 5 shows the combined effect of both resolution and FIR filter length. Increasing the resolution and increasing the FIR filter length both lower the FOM to a value much closer to an analog implementation. An optimum choice is 11 bits with an FIR filter length of 8 samples. Increasing the resolution or FIR length beyond this point results in diminishing effects on the FOM improvement.

Resolution (bits)	Reference (No FIR)	5 Sample avg	8 Sample avg	10 Sample avg	12 Sample avg
10	51.75	40	34.532	34.532	25.9
11	30.22	25.89	21.58	21.58	21.58
12	21.58	17.26	17.26	17.26	15.11
13	17.27	15.1	15.1	15.1	15.11
14	15	14.02	14.02	14.02	14.02
Analog	13.37				

TABLE I
FIR filter FOMs at multiple resolutions for 1 LSB dither (Units are $\frac{ppm}{^oC}$)

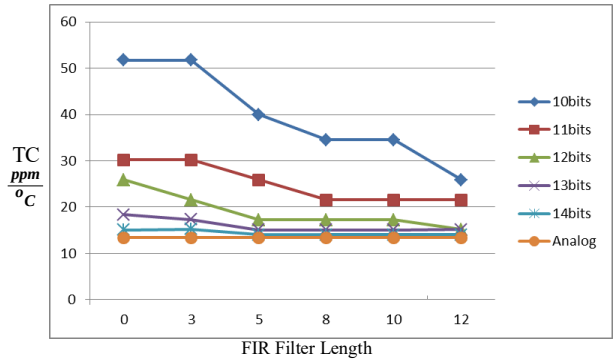

Fig. 5. FOM versus FIR length for several resolutions

APPENDIX A
CURRENT RATIO AND MULTIPLIER (M) RELATIONSHIP

The choice of current ratio is based on a common centroid scheme which increases tolerance to process variations. Given this scheme, the available choices within reasonable limits in area are: 1:1, 1:8, 1:24. A ratio higher than 1:1 is needed to properly create a digitized $\overline{\Delta V_{BE}}$. The discovery is that if the ratios between the currents are not large enough (at least 1:24), a large M (e.g > 7) is required in the digital domain to compensate for the differences in slope magnitude. This leads to larger quantization errors because the scaling of each LSB is proportional to the quantization error. Conversely increasing the ratio facilitates lowering M thereby reducing the quantization error, but this introduces a larger error in ratio in the analog domain. Simulation shows that it is more favorable to keep the large ratio and minimize M.

APPENDIX B
FIR FILTER COMPARISONS

Figure 6 and figure 7 shows show the visual degree of improvement over temperature for different resolutions of multiple FIR filter length.

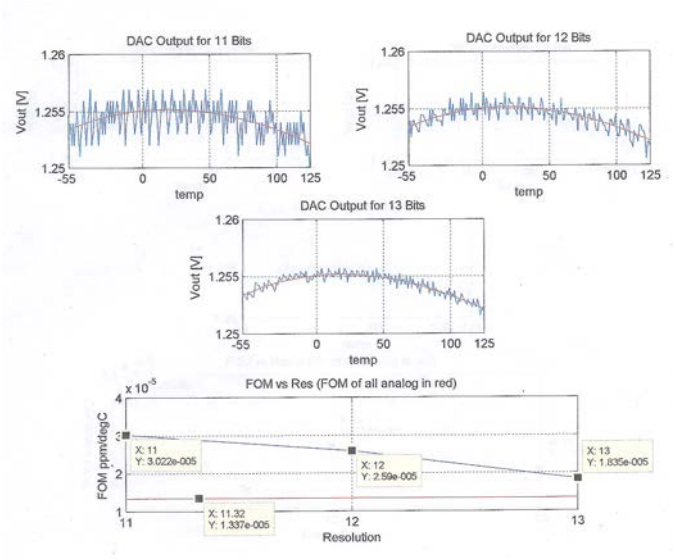

Fig. 6. Output simulation results for Dither = 0 and FIR=0 sample averaging

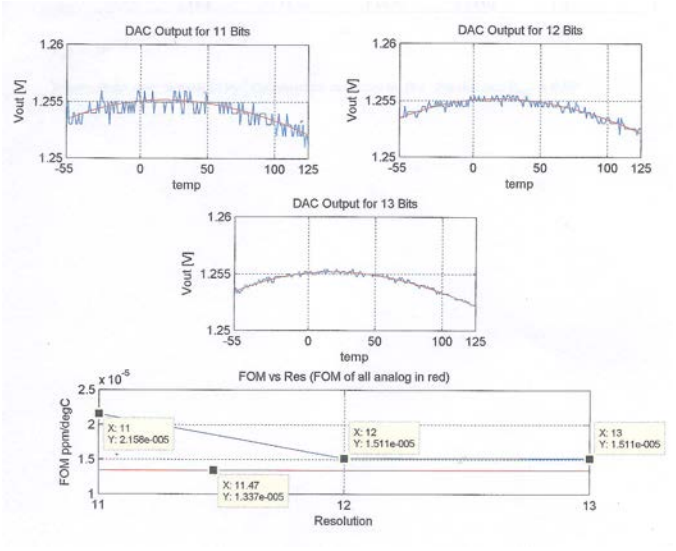

Fig. 7. Output simulation results for Dither = 1LSB and FIR=12 sample averaging

APPENDIX C
ROUNDING

The choice of rounding can affect the final band-gap voltage. The extent of this effect is shown in Figure 8. The temperature range in does not correspond to either military commercial range. The figure is mainly for comparing the rounding types. From the error plot for truncation versus the other error plots, it is apparent that there is a slight bias in the truncated output. Although this error is relatively small, a strict requirement on the band-gap voltage would require that this bias be removed. Convergent rounding would be better in this case (though it may be more expensive to implement).

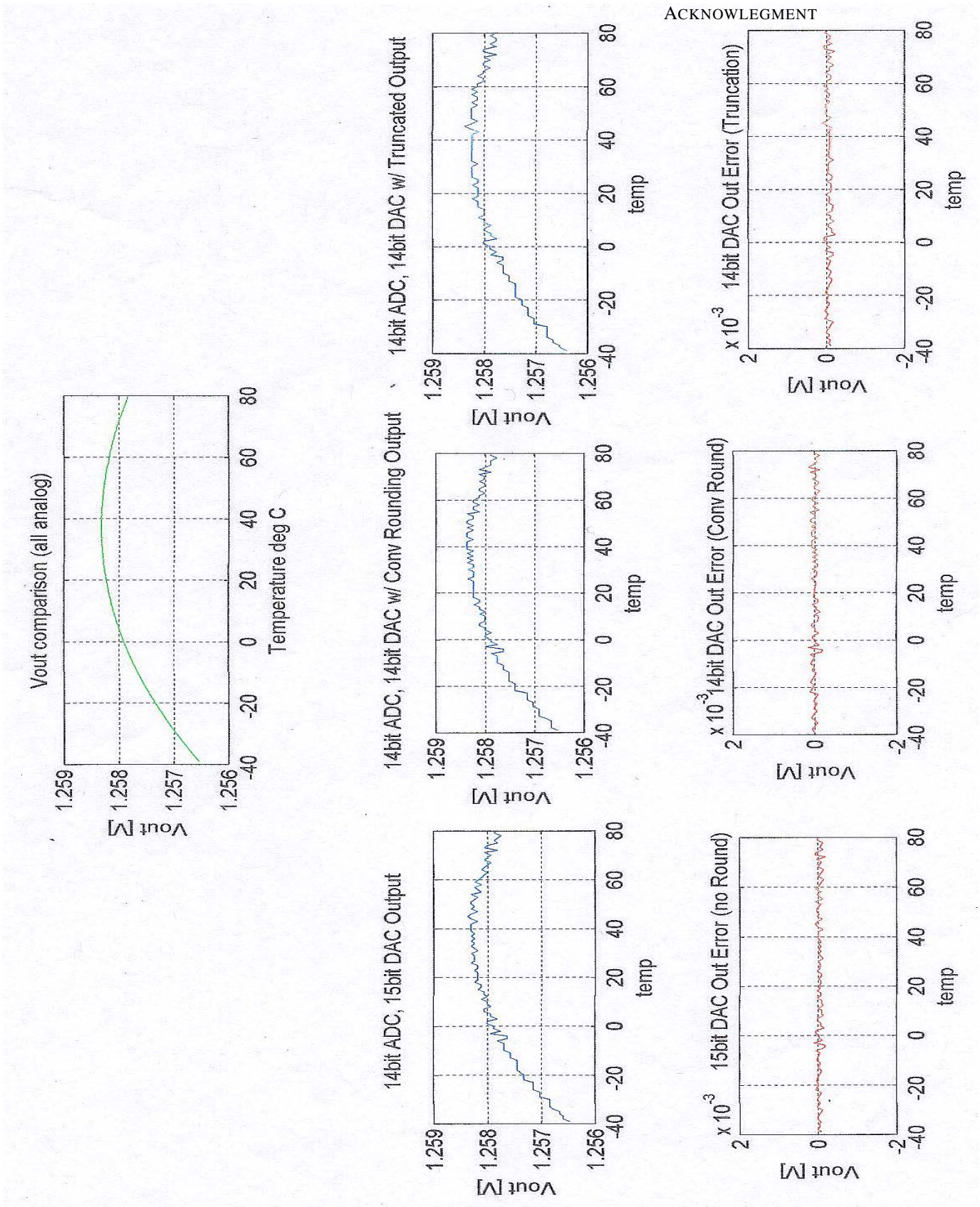

Fig. 8. Rounding comparisons with no dither or FIR

ACKNOWLEGMENT