V. Related Work

Peh *et al.* proposed a speculative technique for VC routers allowing a packet to simultaneously arbitrate for both VCA and SA giving a higher priority for non-speculative packets to win SA; therefore reducing zero-load latency in which the probability of failed speculation is small [13]. This low latency, however, comes with the high complexity of SA circuitry and also wastes more power each time the speculation fails. A packet must stall if even it wins SA but fails VCA, and then has to redo both arbitration at next cycle. Reversely, RoShaQ is non-speculative architecture. An incoming packet in RoShaQ only stalls if it fails both OPA and SQA; therefore it has high chance to advance either to be written to a shared queue (if it wins SQA) or be sent to output port (if it wins OPA) instead of stalling at an input port, and also reducing re-arbitration times.

Increasing crossbar input ports, that allows to directly connect to all virtual-channels of an input port instead of muxing them, improves much network throughput for VC routers. Using a large-radix crossbar is feasible and low-cost than adding more buffers as the results reported by DeMicheli *et al.* [19]. Recently, Passas *et al.* designed a 128×128 crossbar allowing to connect 128 tiles while occupying only 6% of their area [20]. This fact encourages us to build RoShaQ that has two crossbars while sharing cost-expensive buffer queues. The additional costs of crossbars are compensated by the simplicity of allocators and reducing the number of routing computation circuits that make our router better VC routers in many-fold: throughput, latency and packet energy.

IBM Colony router has a shared central buffer which is built from a time-multiplexed multi-bank SRAM array with wide word-width in order that it can be simultaneously written/read multiple flits (defined as a chunk) by input/output ports [21]. As a result, the central buffer is high cost and not identical with input queue design. RoShaQ has all buffer queues (both input and share queues) to be the same structure that allows to reuse the existing generic simple queues reducing practical design and test costs.

Latif *et al.* implemented a router with input ports sharing all queues [10] that is similar to the architecture illustrated in Fig. 6(a). Its implementation on FPGA shows more power and area-efficient than typical input VC routers. However, no router performance was reported and compared to VC routers. A similar approach is proposed by Tran *et al.* [15]; however, due to the high complexity of its allocators and also inter-router round-trip request/grant signaling, its performance is actually poorer than a typical router.

Ramanujam *et al.* recently proposed a router architecture with shared-queues named DSB which emulates an output-buffered router [11]. This router is similar to one illustrated in Fig. 6(b) that has higher zero-load latency than a VC router. This is because a packet has to travel through both two crossbars and be buffered in both input and shared queues at each router. Besides that, the timestamp-based flow control of DSB router design is highly complicated and hence consumes much larger area and power than a typical VC router (that are 35% and 58%, respectively). RoShaQ allows input packets to bypass shared-queues hence achieves lower zero-load latency compared to VC routers. RoShaQ also achieves much higher saturation throughput than VC routers, with only small area and power overheads while consuming less average energy per packet.

VI. Conclusion

We have presented RoShaQ, a new router architecture which allows to share multiple buffer queues for improving network throughput. Input packets also can bypass shared queues to achieve low latency in the case that the network load is low. Compared to a typical VC router, it is 21% lower zero-load latency and 14% higher saturation throughput with only 4% higher power and 16% larger area. It is also 2% higher throughput than a full-crossbar VC router with 3% less than power and area. While targeting the same average packet latency of 60 cycles, RoShaQ has 7% and 5% less energy dissipated per packet than typical VC and full-crossbar VC routers, respectively, while having the same buffer space. Its low latency, high throughput and low energy are achieved without the need of pipeline speculation.

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